WHAT IS CLAIMED IS:

1. A circuit for controlling two switches bidirectional for the voltage and unidirectional for the current, assembled in anti-parallel, comprising, in series between two terminals of the anti-parallel assembly, two identical control stages respectively dedicated to each switch and between which is interposed a common impedance setting a phase angle for the turning-on of the switches, each stage comprising:

a controllable current source for providing a current to a control electrode of the concerned switch;

a capacitor for storing a supply voltage of at least the current source;

an element of activation/deactivation of the current source according to the voltage across the stage capacitor; and

an assembly for discharging the capacitor during the operation of the other stage.

2. The circuit of claim 1, wherein said current source is sized to control the di/dt at the switching-on of the concerned switch.

3. The circuit of claim 1, wherein said discharge assembly is activated as soon as the current in the concerned switch is canceled.

4. The circuit of claim 1, wherein the capacitor of each stage is in series with a first diode, between the impedance and the stage terminal which is the same as the terminal of the anti-parallel assembly.

5. The circuit of claim 4, wherein a second diode of each stage connects said impedance with said terminal of the stage which is the same as the anti-parallel assembly terminal.

6. The circuit of claim 5, wherein a third diode connects the control electrode of the switch of each stage to the electrode of said capacitor, so that said discharge assembly also discharges the control electrode of the stage switch.

7. The circuit of claim 1, wherein the respective capacitor of each stage provides the power supply necessary to all stage components.

8. The circuit of claim 1, wherein said activation/deactivation element activates said current source with which it is associated when the voltage across the capacitor of the stage becomes greater than a first threshold, itself greater than the threshold voltage of the concerned switch.

9. The circuit of claim 8, wherein said comparator deactivates said current source with which it is associated when the voltage across the capacitor of the stage becomes greater than a second threshold, itself preferably smaller than said threshold voltage of the concerned switch.

10. The circuit of claim 1, wherein each discharge assembly comprises a first transistor in parallel with the stage capacitor, the control electrode of the first transistor being connected, via a second transistor, to said impedance.

11. The circuit of claim 1, wherein said activation/deactivation element of each stage is formed of a comparator receiving at a first input the voltage across the stage capacitor and at a second input a reference voltage, said comparator being supplied by the voltage across the capacitor of the concerned stage.

12. The circuit of claim 1, wherein said impedance is formed of a potentiometer.

13. The circuit of claim 1, wherein said impedance is formed of a first resistor in parallel with a second switchable resistor, said first resistor having a much greater value than the second one.

14. A power dimmer of a load, comprising the circuit of claim 1.

15. A circuit for controlling a motor, comprising the circuit of claim 1.

16. A power-reducing circuit, comprising:

a load node;

a supply node operable to receive a time-varying supply signal having a positive half period during which the load node is positive relative to the supply node and having a negative half period during which the load node is negative relative to the supply node;

a first switch coupled to the load node and to the supply node;

a second switch coupled to the load node and the supply node;

a first control stage coupled to the load node and operable to close the first switch during a portion of the positive half period of the supply signal; and

a second control stage serially coupled between the first control stage and the supply node and operable to close the second switch during a portion of the negative half period of the supply signal.

17. The power-reducing circuit of claim 16 wherein the time-varying signal comprises a sinusoidal voltage signal.

18. The power-reducing circuit of claim 16 wherein:

the first control stage is operable to open the first switch when a current through the first switch decays to approximately zero; and

the second control stage is operable to open the second switch when a current through the second switch decays to approximately zero.

19. The power-reducing circuit of claim 16 wherein the first control stage comprises:

a capacitor operable to receive a charging current during the positive half period of the supply signal;

a comparator operable to close the first switch when a voltage across the capacitor exceeds a first reference voltage and to open the first switch when the voltage across the capacitor is less than a second reference voltage; and

a discharge circuit operable to discharge the capacitor when the charging current decays to approximately zero.

20. The power-reducing circuit of claim 16 wherein the second control stage comprises:

a capacitor operable to receive a charging current during the negative half period of the supply signal;

a comparator operable to close the second switch when a voltage across the capacitor exceeds a first reference voltage and to open the second switch when the voltage across the capacitor is less than a second reference voltage; and

a discharge circuit operable to discharge the capacitor when the charging current decays to approximately zero.

21. The power-reducing circuit of claim 16, further comprising an adjustable impedance serially coupled between the first and second control stages.

22. A system, comprising:

first and second supply nodes operable to receive a time-varying supply signal having a positive half period during which the first supply node is positive relative to the second supply node and having a negative half period during which the first supply node is negative relative to the second supply node;

a load having a first node coupled to the first supply node and having a second node; and

a power-reducing circuit coupled between the second node of the load and the second supply node and comprising,

a first switch coupled between the load and the second supply node,

a second switch coupled between the load and the second supply node,

a first control stage coupled to the load and operable to close the first switch during a portion of the positive half period of the supply signal; and

a second control stage serially coupled between the first control stage and the second supply node and operable to close the second switch during a portion of the negative half period of the supply signal.

23. The system of claim 22 wherein the load comprises an inductive load.

24. A method, comprising:

driving a load with a time-varying signal;

charging a first capacitor with a first current that flows through the load during a first portion of the signal;

causing a second current to flow through the load when a voltage across the first capacitor exceeds a first predetermined voltage; and

prohibiting the second current from flowing through the load when the voltage across the first capacitor decays to approximately a second predetermined voltage.

25. The method of claim 24, further comprising adjusting a time that the second current flows through the load by adjusting the first current.

26. The method of claim 24 wherein a total current through the load equals a sum of the first and second currents.

27. The method of claim 24 wherein the second current is significantly greater than the first current.

28. The method of claim 24 wherein:

causing the second current to flow comprises closing a switch in series with the load; and

prohibiting the second current from flowing comprises opening the switch.

29. The method of claim 24 wherein:

causing the second current to flow comprises activating a transistor in series with the load;

prohibiting the second current from flowing comprises deactivating the transistor; and

the second predetermined voltage comprises a threshold of the transistor.

30. The method of claim 24, further comprising:

charging a second capacitor with a third current that flows through the load during a second portion of the signal;

causing a fourth current to flow through the load when a voltage across the second capacitor exceeds a third predetermined voltage; and

prohibiting the fourth current from flowing through the load when the voltage across the second capacitor decays to approximately a fourth predetermined voltage.

31. A method, comprising:

driving a load with a time-varying signal;

charging a capacitor with a first current that flows through a load during a first portion of the signal;

causing a second current to flow through the load when a voltage across the capacitor exceeds a predetermined voltage; and

prohibiting the second current from flowing through the load when the first current decays to approximately a predetermined current.

32. The method of claim 31 wherein the predetermined current equals zero current.